AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) An apparatus for detecting errors on a source-synchronous bus, comprising:

the source-synchronous bus, wherein the source-synchronous bus includes a plurality of data lines and a clock line;

a transmitting mechanism coupled to the source-synchronous bus, wherein the transmitting mechanism is configured to transmit data on the source-synchronous bus;

a receiving mechanism coupled to the source-synchronous bus, wherein the receiving mechanism is configured to receive data from the source-synchronous bus; ~~and~~

an error detecting mechanism coupled to the receiving mechanism that is configured to detect errors on the source-synchronous bus;

a grouping mechanism coupled to the transmitting mechanism that is configured to group data bits into an error group, wherein the grouping mechanism is further configured to skew data bits within the error group across time;

a detection code generating mechanism coupled to the grouping mechanism that is configured to generate a detection code for the error group; and

the transmitting mechanism that is further configured to transmit the detection code on the source-synchronous bus using a clock cycle other than the clock cycles used for transmitting data bits of the error group;

wherein data bits in the error group are transmitted at different times; and

wherein the error detecting mechanism can detect errors on the plurality of data lines including errors that are caused by an error on the clock line.

2. (Canceled).

3. (Currently amended) The apparatus of ~~claim 2~~claim 1, wherein the detection code is a parity bit.

4. (Currently amended) The apparatus of ~~claim 2~~claim 1, wherein the detection code is an error correcting code.

5. (Canceled).

6. (Currently amended) The apparatus of ~~claim 5~~claim 1, wherein skewing data bits across time includes delaying a data bit based on a position of the data bit within the error group.

7. (Currently amended) The apparatus of ~~claim 5~~claim 1, further comprising a gathering mechanism coupled to the receiving mechanism, wherein the gathering mechanism is configured to de-skew data bits within the error group.

8. (Currently amended) A method for detecting errors on a source-synchronous bus, wherein the source-synchronous bus includes a plurality of data lines and a clock line, the method comprising:

grouping data bits into an error group;

skewing data bits within the error group across time;

generating a detection code for the error group;

transmitting data from a source on the source-synchronous bus;

transmitting the detection code on the source-synchronous bus using a clock cycle other than the clock cycles used for transmitting data bits of the error group;

receiving data at a destination from the source-synchronous bus; and

detecting data errors at the destination, wherein detecting data errors includes detecting errors that are caused by errors on the clock line.

9. (Canceled).

10. (Currently amended) The method of ~~claim 9~~claim 8, wherein the detection code is a parity bit.

11. (Currently amended) The method of ~~claim 9~~claim 8, wherein the detection code is an error correcting code.

12. (Canceled).

13. (Currently amended) The method of ~~claim 12~~claim 8, wherein skewing data bits across time includes delaying a data bit based on a position of the data bit within the error group.

14. (Currently amended) The method of ~~claim 12~~claim 8, further comprising de-skewing data bits within the error group.

15. (Currently amended) A computing system for detecting errors on a source-synchronous bus, comprising:

the source-synchronous bus, wherein the source-synchronous bus includes a plurality of data lines and a clock line;

a central processing unit coupled to the source-synchronous bus, wherein the central processing unit is configured to transmit data on the source-synchronous bus;

a memory unit coupled to the source-synchronous bus, wherein the memory unit is configured to receive data from the source-synchronous bus;

an error detecting mechanism coupled to the memory unit that is configured to detect errors on the source-synchronous bus;

a grouping mechanism coupled to the transmitting mechanism that is configured to group data bits into an error group, wherein the grouping mechanism is further configured to skew data bits within the error group across time;

a detection code generating mechanism coupled to the grouping mechanism that is configured to generate a detection code for the error group; and

the transmitting mechanism that is further configured to transmit the detection code on the source-synchronous bus using a clock cycle other than the clock cycles used for transmitting data bits of the error group;

wherein data bits in the error group are transmitted at different times; and

wherein the error detecting mechanism can detect errors on the plurality of data lines including errors that are caused by an error on the clock line.

16. (Canceled).

17. (Currently amended) The computing system of ~~claim 16~~claim 15, wherein the detection code is a parity bit.

18. (Currently amended) The computing system of ~~claim 16~~claim 15, wherein the detection code is an error correcting code.

19. (Canceled).

20. (Currently amended) The computing system of ~~claim 19~~claim 15, wherein skewing data bits across time includes delaying a data bit based on a position of the data bit within the error group.

21. (Currently amended) The computing system of ~~claim 19~~claim 15, further comprising a gathering mechanism coupled to the memory unit, wherein the gathering mechanism is configured to de-skew data bits within the error group.